

AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior versions, and all prior listings, of claims in the application.

Listing of Claims:

Claim 1. (Cancelled)

2. (New) A process for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a metal layer including copper as its principal component over an insulating film over a first major surface of a wafer, the insulating film having a wiring groove pattern;

(b) removing the metal layer outside the wiring groove pattern by a chemical mechanical polishing method so as to leave the metal layer in the wiring groove pattern, said removing being performed in a chemical mechanical polishing section of a single wafer processing apparatus;

(c) after step (b), transferring the wafer to a post cleaning section of the single wafer processing apparatus, while keeping the first major surface of the wafer wet with moving water;

(d) performing scrub or brush cleaning to the first major surface of the wafer with a liquid chemical or pure water in the post cleaning section; and

(e) after step (d), making the first major surface of the wafer dry,

wherein the single wafer processing apparatus has a light shielding structure enclosing the post cleaning section and between the chemical mechanical polishing section and the post cleaning section.

3. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 2, wherein the moving water is a water shower.

4. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 3, wherein the metal layer left in the wiring groove pattern in step (b) constitutes a portion of a metal wiring of a dual damascene wiring.

5. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 4, wherein step (d) is performed prior to a substantial progress of corrosion of the metal layer left in the wiring groove pattern.

6. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 5, wherein the first major surface of the wafer is kept wet from the end of step (b) to the end of step (d).

7. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 6, wherein the moving water is a pure water shower.

8. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 2, wherein step (a) includes the substep of:

(i) forming the metal layer including copper as its principal component over an upper surface of the insulating film and inside the wiring groove pattern by electroplating.

9. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 2, wherein the metal layer left in the wiring groove pattern in step (b) constitutes a portion of a metal wiring of a dual damascene wiring.

10. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 2, wherein the first major surface of the wafer is kept wet from the end of step (b) to the end of step (d).

11. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 3, wherein the light shielding structure includes a light shielding sheet.

12. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 4, wherein the light shielding structure includes a light shielding sheet.

13. (New) A process for manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a metal layer over an insulating film over a first major surface of a wafer, the insulating film having first and second wiring groove patterns;

(b) removing the metal layer outside the first and second wiring groove patterns by a chemical mechanical polishing method so as to leave the metal layer in the first and second wiring groove patterns and thereby electrically dividing metal wiring members inside the first and second wiring groove patterns, said removing being performed in a chemical mechanical polishing section of a single wafer processing apparatus;

(c) after step (b), transferring the wafer to a post cleaning section of the single wafer processing apparatus, while keeping the first major surface of the wafer wet with moving water;

(d) performing scrub or brush cleaning to the first major surface of the wafer with a liquid chemical or pure water in the post cleaning section; and

(e) after step (d), making the first major surface of the wafer dry,

wherein the single wafer processing apparatus has a light shielding structure enclosing the post cleaning section and between the chemical mechanical polishing section and the post cleaning section.

14. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 13, wherein the moving water is a water shower.

15. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 14, wherein portions of the metal layer left inside the first and second wiring groove patterns in step (b) constitute portions of metal wiring members of a dual damascene wiring.

16. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 15, wherein step (d) is performed prior to a substantial progress of corrosion of the metal layer left in the first and second wiring groove patterns.

17. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 16, wherein the first major surface of the wafer is kept wet from the end of step (b) to the end of step (d).

18. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 17, wherein the moving water is a pure water shower.

19. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 13, wherein portions of the metal layer left inside the first and second wiring groove patterns in step (b) constitute portions of metal wiring members of a dual damascene wiring.

20. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 13, wherein step (d) is performed prior to a substantial progress of corrosion of the metal layer left in the first and second wiring groove patterns.

21. (New) A process for manufacturing a semiconductor integrated circuit device according to Claim 13, wherein the first major surface of the wafer is kept wet from the end of step (b) to the end of step (d).